Atmel SAM4S-WPIR-RD

User Guide

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Section 1
Introduction

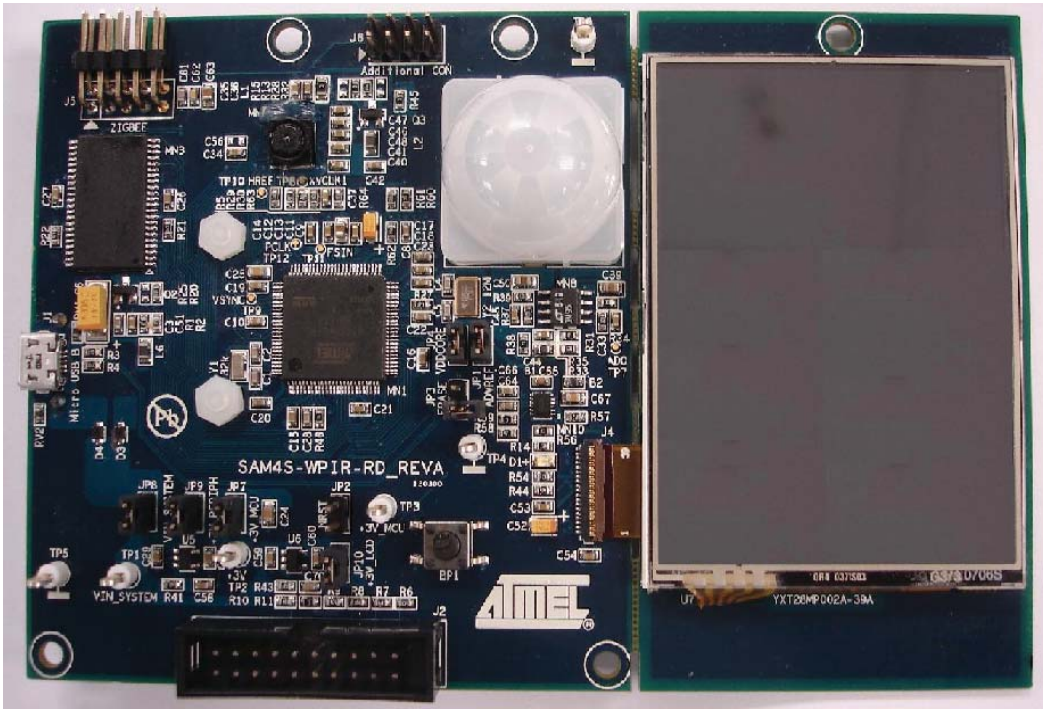
1.1 Scope

The SAM4S-WPIR-RD Reference Design Kit is based on SAM4S16C device. It introduces the application of Passive InfraRed Motion Detector Camera.

This User Guide gives design details on the Reference Design Kit and is made up of 4 sections:

- Section 1 includes a photo of the board, references and applicable documents.
- Section 2 describes the contents and the main features of the Reference Design Kit.
- Section 3 provides instructions to power up the board and describes how to use it.
- Section 4 describes the hardware resources, function blocks, connectors and schematics.

Figure 1-1. Board Photo



1.2 References and Applicable Documents

Table 1-1. References and Applicable Documents

Title	Comment
SAM4S datasheet	http://www.atmel.com/products/microcontrollers/arm/sam4s.aspx?tab=documents

Section 2
Kit Contents

2.1 Deliverables

The Atmel® SAM4S-WPIR-RD Reference Design Kit includes:

- Board
  - One SAM4S-WPIR-RD board
- Power supply
  - USB supply
- Cables
  - One USB cable, type A to type Micro-B

Unpack and inspect the kit carefully. Contact your local Atmel distributor, should there be issues concerning the contents of the kit.

2.2 Board Specifications

Table 2-1. SAM4S-WPIR-RD Board Specifications

Characteristics	Specifications
Clock speed	48 MHz MCK
Ports	USB, JTAG
Board supply voltage	5V DC from USB or 3 x AAA Alkaline cells
Temperature - operating - storage	 -10° to +50° C -40° to +85° C
Relative humidity	0 to 90% (non condensing)
Dimensions	136 mm x 90mm
RoHS status	Compliant

2.3 Electrostatic Warning

The SAM4S-WPIR-RD board is shipped in a protective anti-static package. The board system must not be subjected to high electrostatic potentials. A grounding strap or similar ESD protective device should be worn when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

Section 3
Power Up

3.1 Power Up the Board

Unpack the board taking care to avoid electrostatic discharge. Connect the board to PC with the USB cable, or insert 3 x AAA Alkaline cells on U4 Battery Holder, and then the board should be powered on.

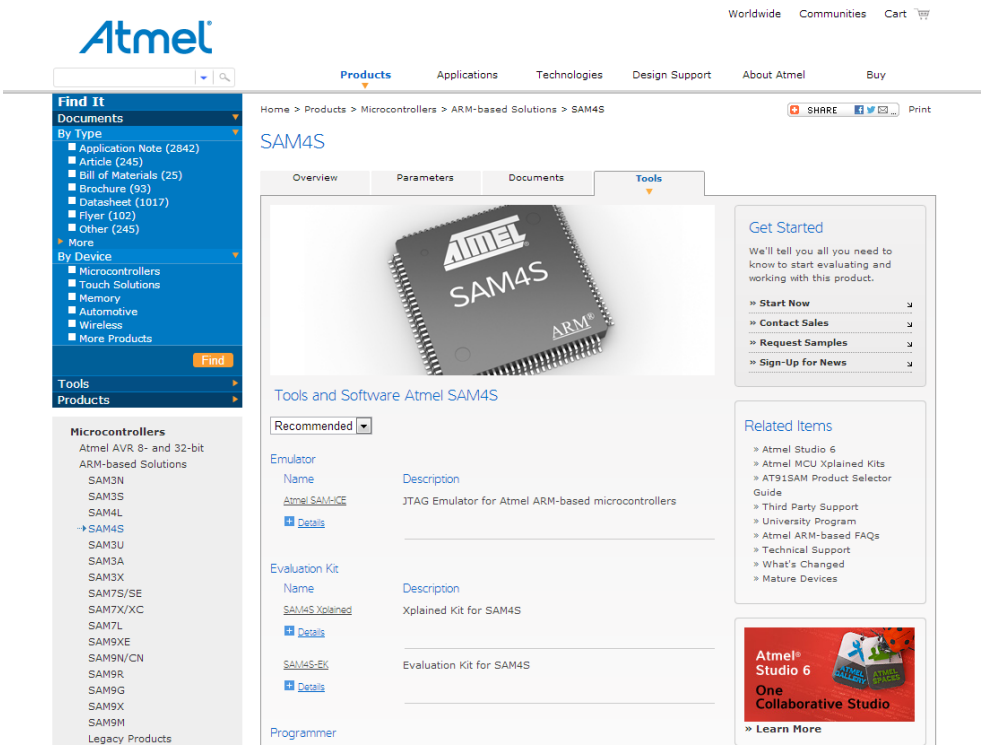
Note: Jumpers JP1, JP4, JP7, JP8, JP9, JP10 must be closed and JP2, JP3 must be open for start-up.

3.2 Sample Code and Technical Support

Users can download sample code and get technical support from the Atmel web site:

http://www.atmel.com/products/microcontrollers/arm/sam4s.aspx?tab=tools

Figure 3-1. Atmel Web Site for SAM4S Products

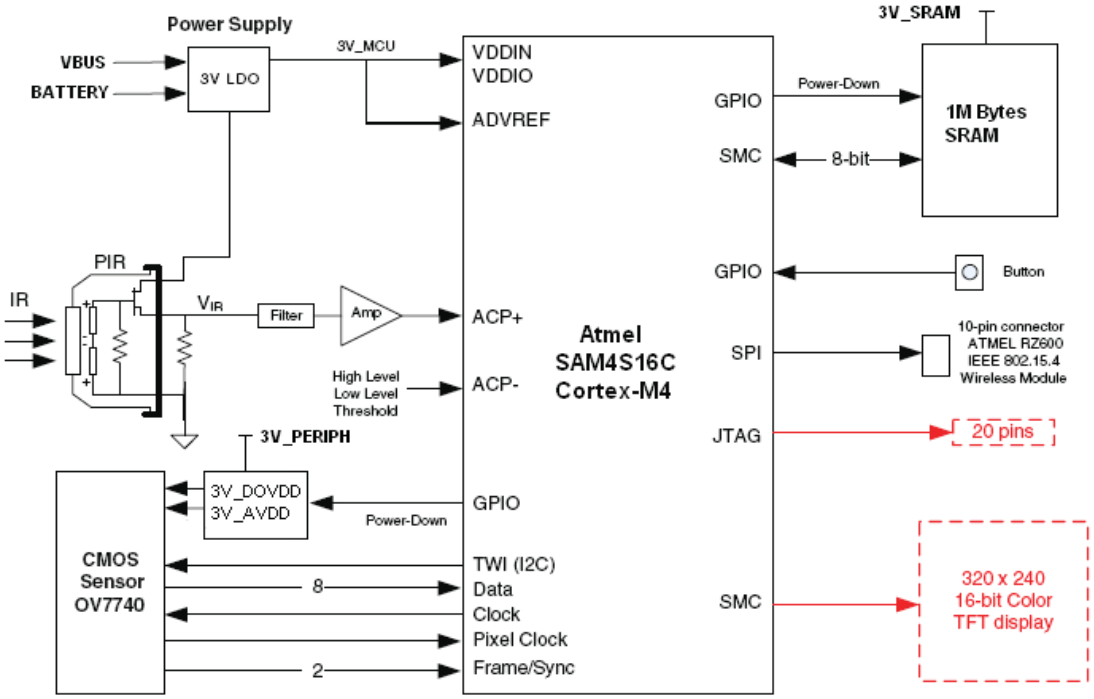


Section 4
Hardware

4.1 Introduction

The SAM4S-WPIR-RD block diagram includes battery holder, LDO, image sensor, 1M byte SRAM, PIR sensor, JTAG connector, LCD, ZigBee connector, as shown in Figure 4-1.

Figure 4-1. SAM4S-WPIR-RD Block Diagram



4.2 Function Blocks

4.2.1 Processor

The board is equipped with a SAM4S16 device in a LQFP100 package.

4.2.2 Clock Circuitry

The board includes 2 clock sources:

- One 12 MHz Crystal for Internal Clock (Y2)
- One 32.768 kHz Crystal for RTC Clock (Y1)

4.2.3 Reset Circuitry

The reset sources for the board are:

- Power on reset
- JTAG reset from an in-circuit emulator (JTAG interface is equipped on the board)

4.2.4 Push Button Switches

- User interface (BP1)

4.2.5 Power Supplies

The Board is driven by 5V input power rail from USB cable or 3 x AAA battery.

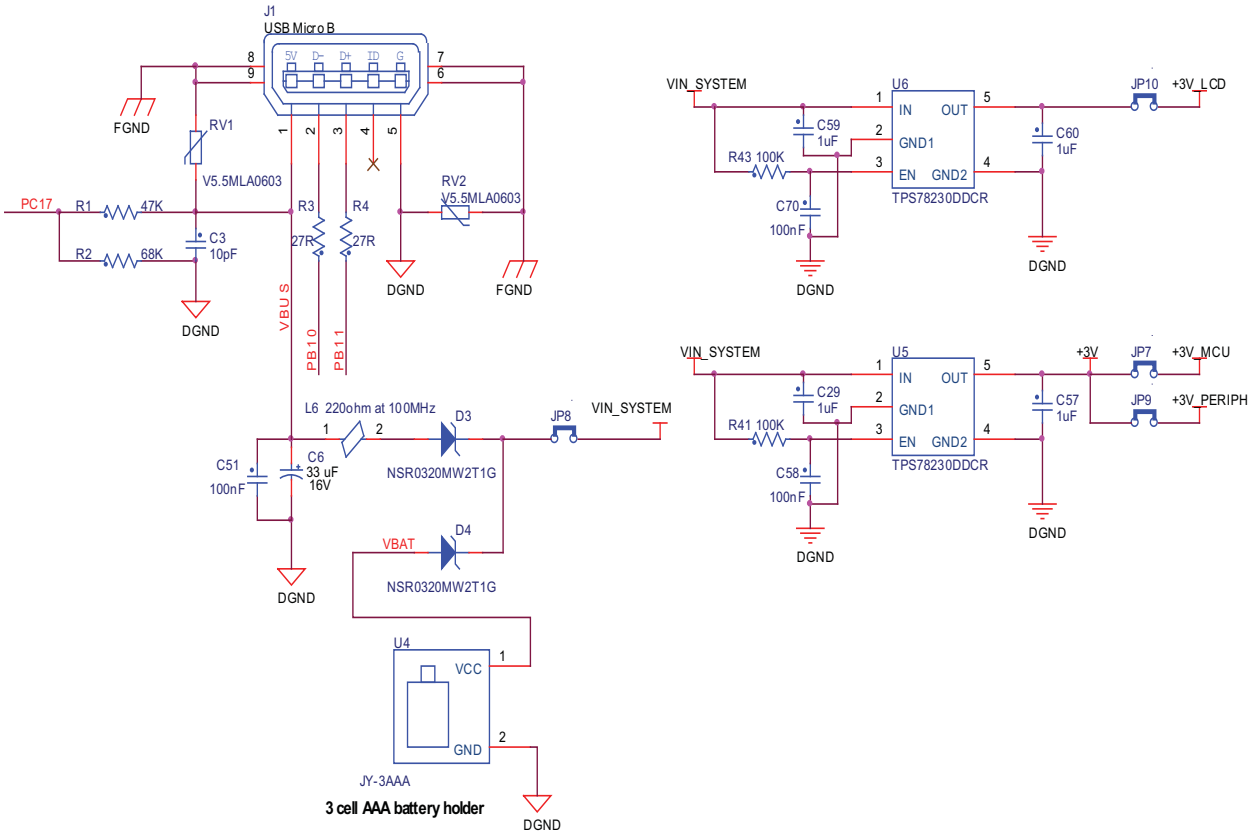
The Board embeds all the necessary power rails required for the microcontroller

Table 4-1 summarizes the power specifications.

Table 4-1. Power Rails Associated with the Systems

Nominal	Name	Powers	Component
3.0V	VDDIO	Partial Peripheral I/O lines	on board
3.0V	+3V_PERIPH	SRAM and image sensor	on board
3.0V	+3V_LCD	LCD and backlight driver	on board
1.2V	VDDPLL	the PLL cell	From SAM4S internal LDO
1.2V	VDDCORE	the core, including the processor, the embedded memories and the peripherals	From SAM4S internal LDO
3.0V	ADVREF	analog	on board

Figure 4-2. Power Supply

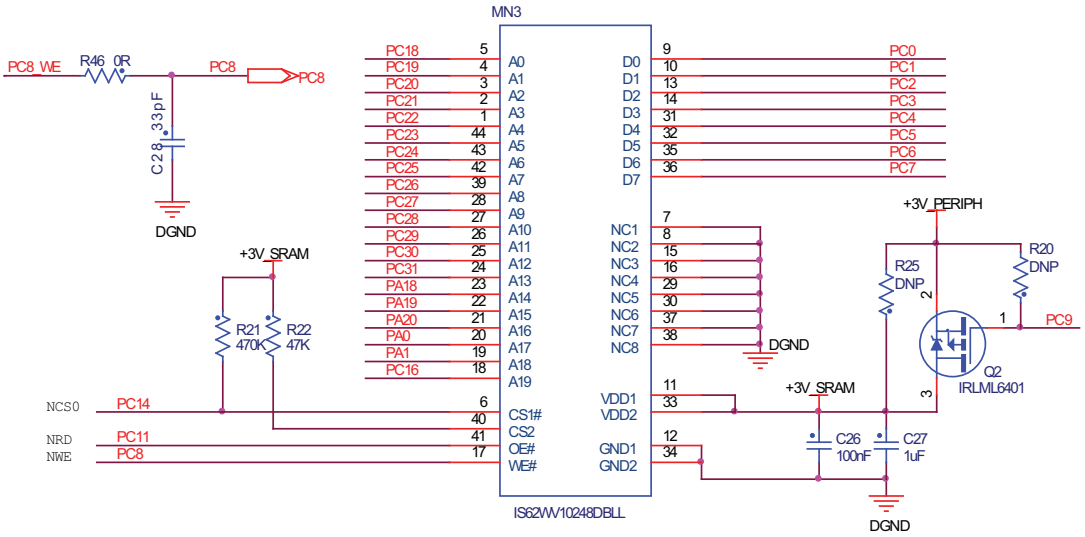


4.2.6 Memory

The SAM4S features an External Bus Interface (EBI) that permits interfacing to a broad range of external memories and virtually to any parallel peripheral. The SAM4S-WPIR-RD board is equipped with a memory device connected to the SAM4 EBI:

- One SRAM IS62WV10248DBLL

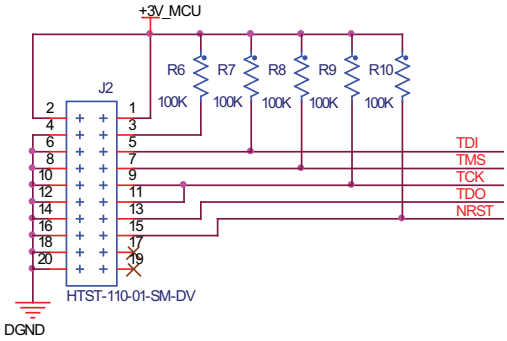
Figure 4-3. Memory



4.2.7 JTAG/ICE

Software debug is accessed by a standard 20-pin JTAG connection. This allows connection to a standard USB-to-JTAG in-circuit emulator such as SAM-ICE™.

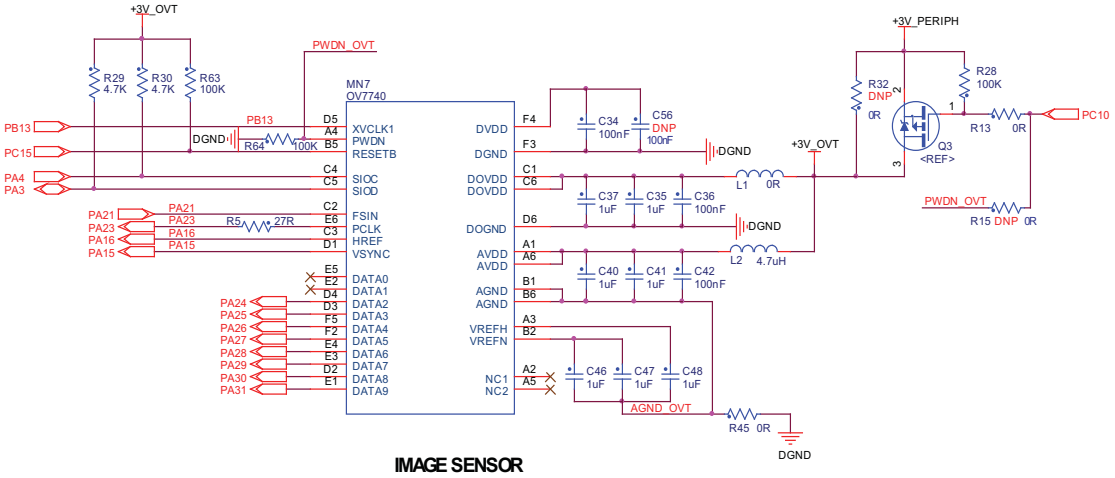
Figure 4-4. JTAG Interface



4.2.8 Image Sensor

The CMOS image sensor, OV7740 from OmniVision, used in this reference design is a low-complexity, low-cost, low-power, yet powerful sensor. It supports VGA (640x480) at up to 60 fps and QVGA (320x240) at up to 120 fps. The OV7740 has standard interface output pins such as data, horizontal/vertical synchronization signals, pixel clock output and main clock input. Interfacing between the CMOS image sensor and the SAM4S device is made easy by means of the sensor interface (parallel capture mode). The SAM4S is able to sample data from the CMOS image sensor without CPU intervention and transfer image data into internal or external memory.

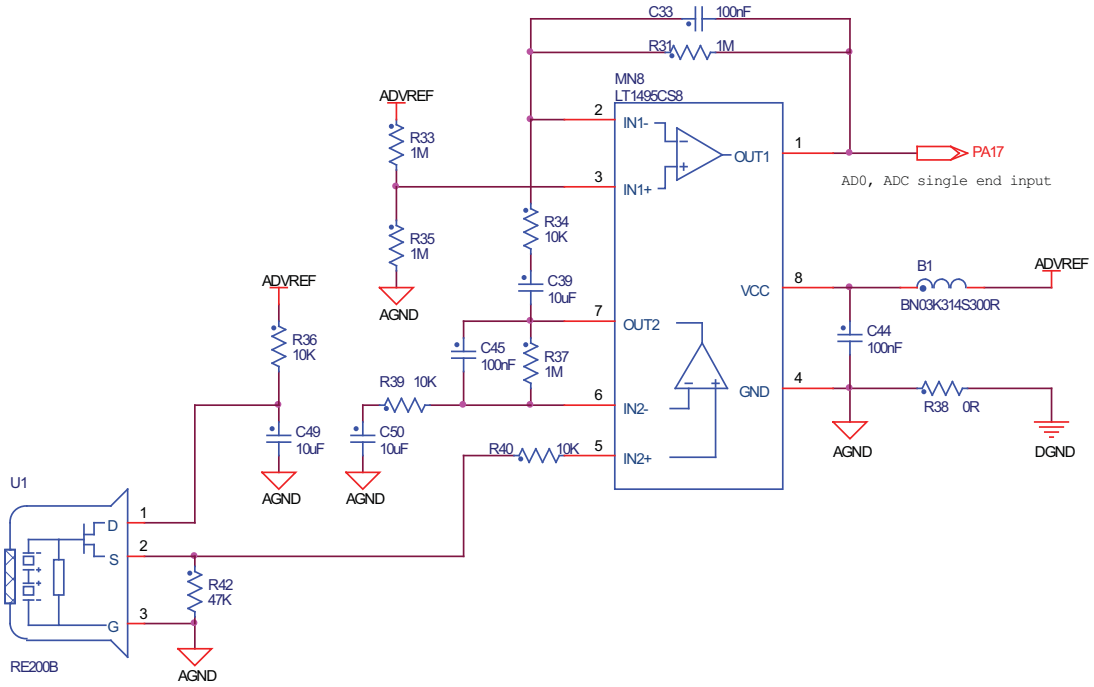
Figure 4-5. Image Sensor



4.2.9 PIR sensor

The PIR sensor (RE200B from Nicera) chosen for the reference design is a general purpose dual element. This model satisfies user's cost reduction needs, keeping most dual element type performances at reasonable levels.

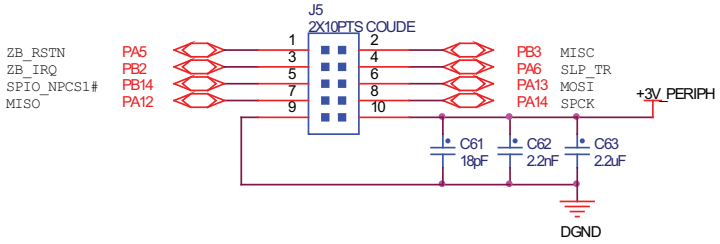
Figure 4-6. PIR Sensor



4.2.10 ZigBee

The board has a 10-pin male connector for the Atmel RZ600 ZigBee module.

Figure 4-7. ZigBee Interface



4.2.11 LED Indicators

The board has one LED indicator for purposes shown below:

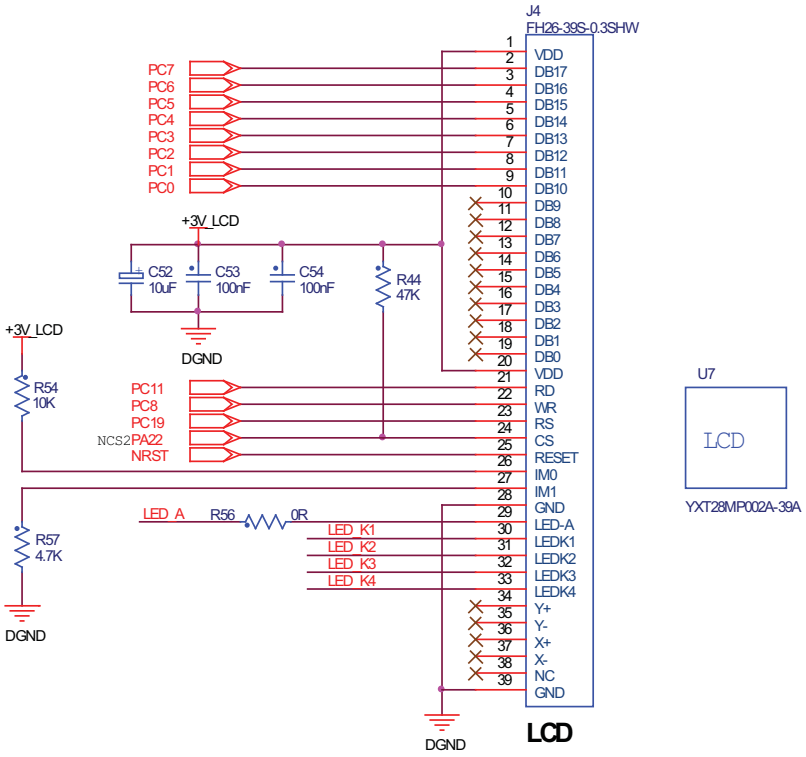
Table 4-2. LED Indicators

Reference	Color	Function
D1	Blue	PIR indicator

4.2.12 LCD

The LCD module gets reset from the NRST signal. As explained, this NRST is shared with the JTAG port. The LCD chip select signal is connected to NCS2. The SAM4S communicates with the LCD through PIOC where an 8-bit parallel “8080-like” protocol data bus has to be implemented by software.

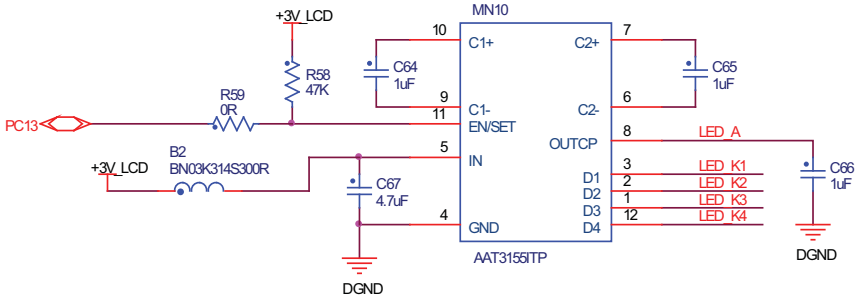
Figure 4-8. LCD Block



4.2.13 Backlight Control

The LCD backlight is made of four integrated white chip-LEDs arranged in parallel. These are driven by an AAT3155 charge pump, MN10.The AAT3155 is controlled by the SAM4S through a single PIO line PC13 interface; the 0 Ohm resistor R59 is mounted in series on this line, which permits to use it for other custom purposes. In that case, the pull-up resistor R58 maintains the charge pump permanently enabled by default.

Figure 4-9. Backlight Control



4.3 Connectors

4.3.1 JTAG/ICE Connector

Figure 4-10. JTAG J2

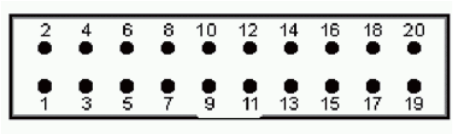


Table 4-3. JTAG/ICE Connector J2 Signal Descriptions

Pin	Mnemonic	Description
1	VTref. 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply. 3.3V power	This pin is not connected in SAM-ICE. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST TARGET RESET - Active-low output signal that resets the target	JTAG Reset. Output from SAM-ICE to the Reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled HIGH on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground
5	TDI TEST DATA INPUT - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground
7	TMS TEST MODE SELECT	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground
9	TCK TEST CLOCK - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.

Pin	Mnemonic	Description
10	GND	Common ground
11	RTCK - Input Return test clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To assist in meeting this requirement, a returned and retimed TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Common ground
13	TDO JTAG TEST DATA OUTPUT - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground
15	nSRST RESET	Active-low reset signal. Target CPU reset signal.
16	GND	Common ground
17	RFU	This pin is not connected in SAM-ICE.
18	GND	Common ground
19	RFU	This pin is not connected in SAM-ICE.
20	GND	Common ground

4.3.2 USB Micro AB

Figure 4-11. USB Device Micro-B Connector J1

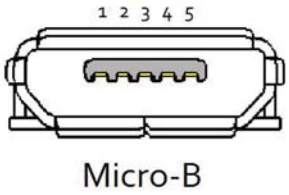


Table 4-4. USB Device Micro-B Connector J1 Signal Descriptions

Pin	Mnemonic	Description
1	Vbus	5v power
2	DM	Data minus
3	DP	Data plus
4	ID	Not used
5	GND	Common ground

4.3.3 ZigBee Socket J5

Figure 4-12. ZigBee Socket J5

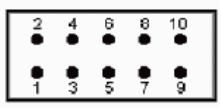


Table 4-5. ZigBee Socket J5 Signal Descriptions

Function	Signal Name	Port	Pin	Pin	Port	Signal Name	Function
Reset	/RST		1	2		Misc.	Interrupt Request
Interrupt Request	IRQ1		3	4		SLP_TR	SLP_TR
SPI chip select	/SEL		5	6		MOSI	SPI MOSI
SPI MISO	MISO		7	8		SCLK	SPI CLK
Power Supply	GND	GND	9	10	VCC	VCC	VCC

4.3.4 LCD/TSC Socket J4

Figure 4-13. LCD/TSC Socket J4

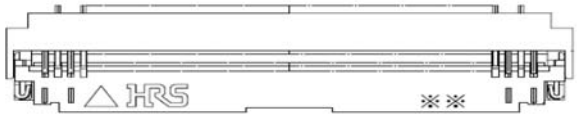
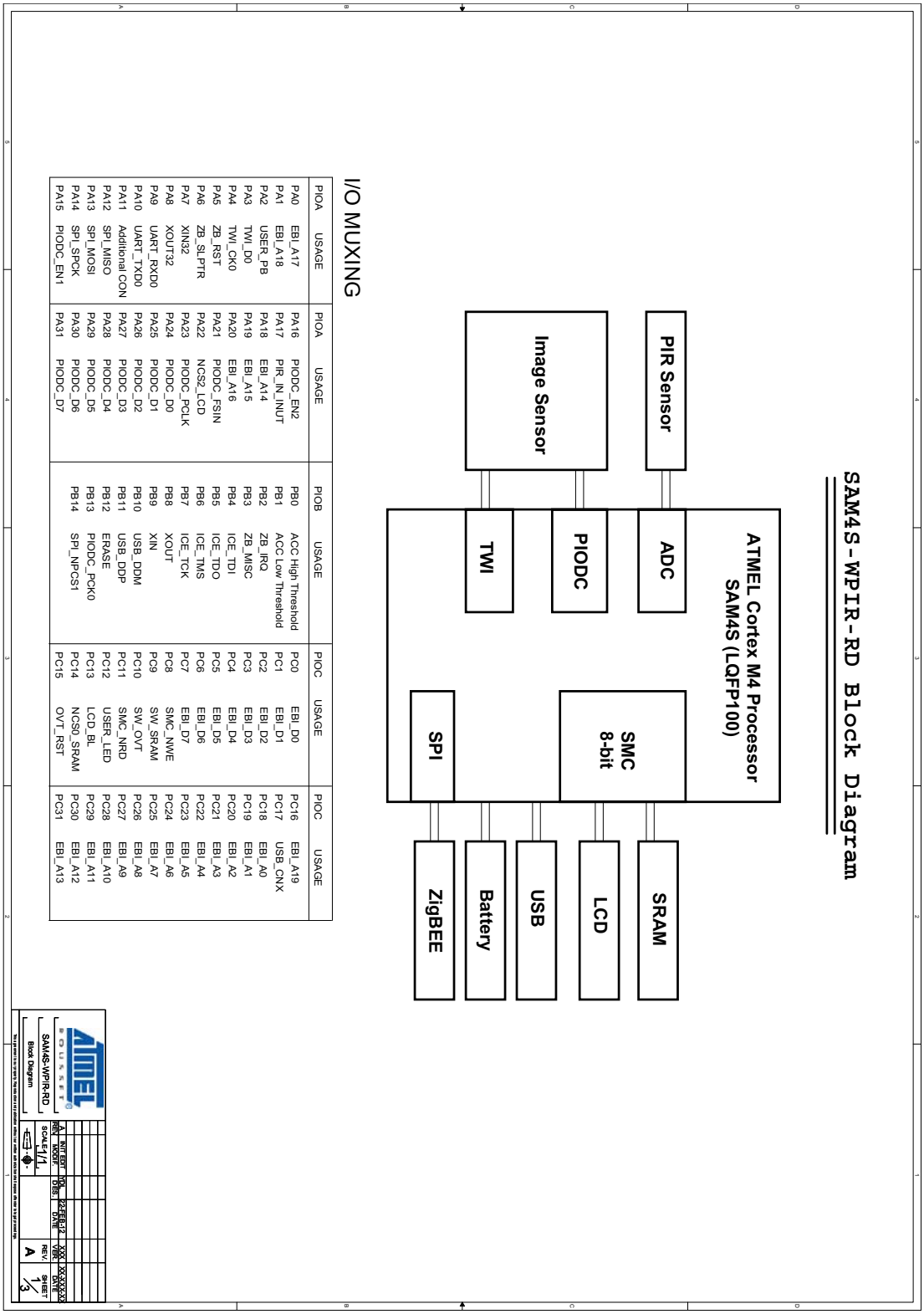


Table 4-6. LCD/TSC Socket J4 Signal Descriptions

Mnemonic		Pin Num	Pin Num	Mnemonic	
VDD	3V_INTER	1	2	PC7	LCDDAT17
LCDDAT16	PC6	3	4	PC5	LCDDAT15
LCDDAT14	PC4	5	6	PC3	LCDDAT13
LCDDAT12	PC2	7	8	PC1	LCDDAT11
LCDDAT10	PC0	9	10	NC	LCDDAT09
LCDDAT08	NC	11	12	NC	LCDDAT07
LCDDAT06	NC	13	14	NC	LCDDAT05
LCDDAT04	NC	15	16	NC	LCDDAT03
LCDDAT02	NC	17	18	NC	LCDDAT01
LCDDAT00	NC	19	20	3V	VDD

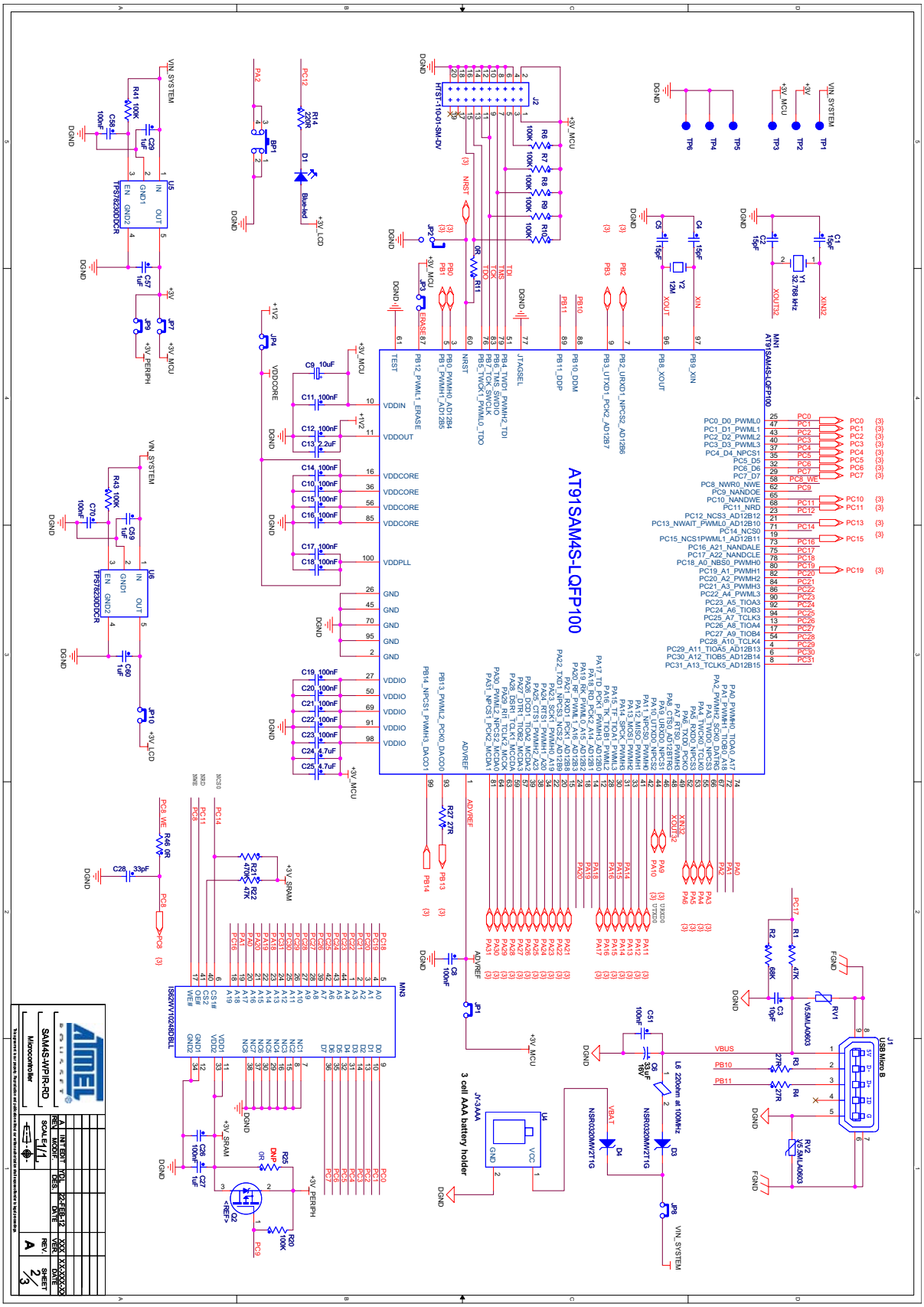
Mnemonic		Pin Num	Pin Num	Mnemonic	
RD	PC11	21	22	PC8	WR
RS	PC19	23	24	PA22	CS
RESET	NRST	25	26	PULL UP	IM0
IM1	PULL DOWN	27	28	GND	GND
LED-A	LED-A	29	30	LED-K1	LED-K1
LED-K2	LED-K2	31	32	LED-K3	LED-K3
LED-K4	LED-K4	33	34	NC	Y UP
Y DOWN	NC	35	36	NC	X RIGHT
X LEFT	NC	37	38	NC	NC
GND	GND	39			

4.4 Schematics



I/O MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE
PA0	EBI_A17	PA16	PIODC_EN2	PB0	ACC High Threshold	PC0	EBI_D0	PC16	EBI_A19
PA1	EBI_A18	PA17	PIR_IN_INUT	PB1	ACC Low Threshold	PC1	EBI_D1	PC17	USB_CNX
PA2	USER_PB	PA18	EBI_A14	PB2	ZB_IRQ	PC2	EBI_D2	PC18	EBI_A0
PA3	TWI_D0	PA19	EBI_A15	PB3	ZB_MISC	PC3	EBI_D3	PC19	EBI_A1
PA4	TWI_CK0	PA20	EBI_A16	PB4	ICE_TDI	PC4	EBI_D4	PC20	EBI_A2
PA5	ZB_RST	PA21	PIODC_FSIN	PB5	ICE_TDO	PC5	EBI_D5	PC21	EBI_A3
PA6	ZB_SLPTR	PA22	NCS2_LCD	PB6	ICE_TMS	PC6	EBI_D6	PC22	EBI_A4
PA7	XIN32	PA23	PIODC_PCLK	PB7	ICE_TCK	PC7	EBI_D7	PC23	EBI_A5
PA8	XOUT32	PA24	PIODC_D0	PB8	XOUT	PC8	SMC_NWE	PC24	EBI_A6
PA9	UART_RXD0	PA25	PIODC_D1	PB9	XIN	PC9	SW_SRAM	PC25	EBI_A7
PA10	UART_TXD0	PA26	PIODC_D2	PB10	USB_DDM	PC10	SW_OVT	PC26	EBI_A8
PA11	Additional CON	PA27	PIODC_D3	PB11	USB_DDP	PC11	SMC_NRD	PC27	EBI_A9
PA12	SPI_MISO	PA28	PIODC_D4	PB12	ERASE	PC12	USER_LED	PC28	EBI_A10
PA13	SPI_MOSI	PA29	PIODC_D5	PB13	PIODC_PCK0	PC13	LCD_BL	PC29	EBI_A11
PA14	SPI_SPCK	PA30	PIODC_D6	PB14	SPI_NPCS1	PC14	NCS0_SRAM	PC30	EBI_A12
PA15	PIODC_EN1	PA31	PIODC_D7			PC15	OVT_RST	PC31	EBI_A13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MN1
AT91SAM4S-LQFP100
MN3
IS62WV10248DBLL
J1
USB Micro B
J2
HTST-110-01-SM-DV
J3
3 cell AAA battery holder
U4
U5
TPS78230DDCR
U6
TPS78230DDCR
U7
VIN_SYSTEM
DGND
+3V_MCU
+3V_LCD
+3V_PERIPH
+3V_SRAM
FGND
SAM4S-WPIR-RD
Microcontroller
SCALE 1/1
REV. A
SHEET 2/3

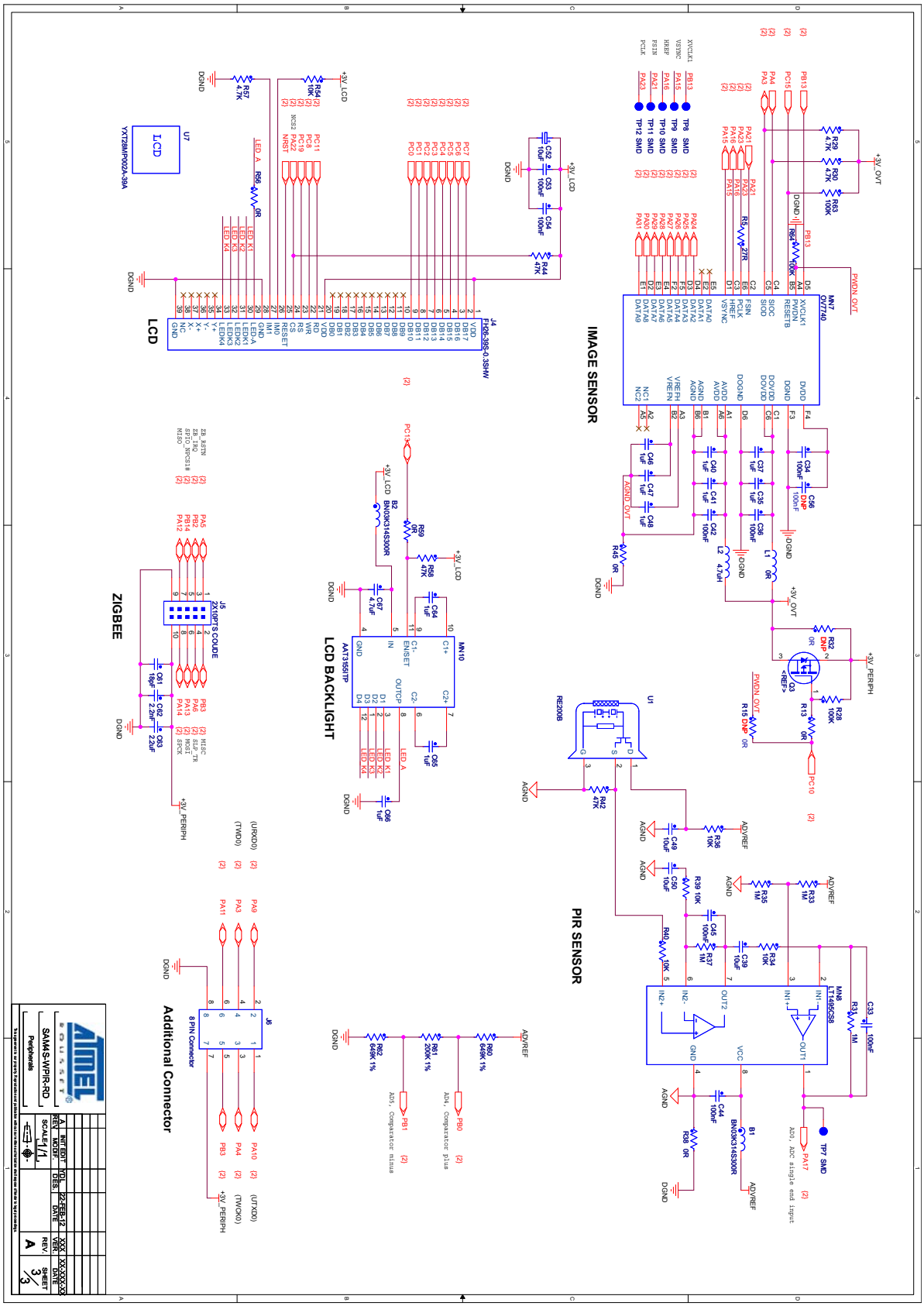
IMAGE SENSOR
PIR SENSOR
LCD BACKLIGHT
ZIGBEE
LCD
Additional Connector
8 PIN Connector
SAM4S-WPIR-RD
Peripherals
A
3
3

Section 5
Revision History

5.1 Revision History

Document	Comments
42060A	Initial

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